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PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY
(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION See Form PCT/IPEA/416	
P35826-P0		
International application No.	International filing date (*day/month/year*)	Priority date (*day/month/year*)
PCT/JP2004/016575	09 November 2004	11 November 2003
International Patent Classification (IPC) or national classification and IPC Int. Cl.[7]		
G11B20/10, 20/14, H03H17/02, 17/06, 21/00		
Applicant		
Matsushita Electric Industrial Co., Ltd.		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 4 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:

a ☒ *(sent to the applicant and to the International Bureau)* a total of 4 sheets, as follows:

☒ sheets of the description, claims and /or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).

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4. This report contains indications relating to the following items:

- ☒ I Basis of the report
- ☐ II Priority
- ☐ III Non-establishment of opinion with regard to novelty, inventive step or industrial applicability
- ☐ IV Lack of unity of invention
- ☒ V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ VI Certain documents cited
- ☐ VII Certain defects in the international application
- ☐ VIII Certain observations on the international application

Date of submission of the demand	Date of completion of this report
30 March 2005	08 November 2005
Name and mailing address of the IPEA/JP Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

ATTACHMENT F

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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/JP2004/016575

I . Basis of the report

1. With regard to the language, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

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2. With regard to the elements of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed " and are not annexed to this report)*:

☒ the description:
pages 1, 2, 4-16, as originally filed/furnished
pages 3, 3/1, received by this Authority on 30 March 2005

☒ the claims:
Nos. 3-10, as originally filed/furnished
Nos. 1, 2, received by this Authority on 30 March 2005

☒ the drawings:
figures 1-11, as originally filed/furnished

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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No. PCT/JP2004/016575

V. Reasoned statement under Rule 12 (PCT Article 35(2)) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. STATEMENT

Novelty (N)	Claims 1-10	YES
	Claims NONE	NO
Inventive Step(IS)	Claims 3-10	YES
	Claims 1, 2	NO
Industrial Applicability (IA)	Claims 1-10	YES
	Claims NONE	NO

2. CITATIONS AND EXPLANATIONS (Rule70.7)

Reference 1: JP 2002-269925 A (Matsushita Electric Industrial Co., Ltd.) 2002.09.20, Paragraphs [0051], [0054]-[0056] & US 2003/0137912 A1

Reference 2: JP 10-214458 A (Matsushita Electric Industrial Co., Ltd.) 1998.08.11, Paragraphs [0007], [0031], [0032] (no family)

Reference 3: JP 2003-178529 A (Koninklijke Philips Electronics N.V.) 2003.06.27, Paragraphs [0032]-[0033], [0039]-[0041], [0051], [0052], Figs. 6, 13, & EP 0585991 A1

Reference 4: JP 9-320198 A (Hitachi, Ltd.) 1997.12.12, Paragraphs [0018], [0039]-[0045] (no family)

Reference 5: JP 2-260876 A (Toshiba Corporation) 1990.10.23, Page 4, upper right column, lines 9-16, Page 4, lower right column, lines 2-10 (no family)

Reference 6: JP 2-109436 A (Nippon Telegraph and Telephone Corporation) 1990.04.23, Claim 1 (no family)

The invention as defined in Claim 1 has no inventive step in view of References 1-3 cited in the International Search Report.

Reference 1 describes the FIR filter that varies a filter coefficient, the equalization error detector 28 that detects an equalization error (which corresponds to the equalizing performance detecting unit), and the correlator 29, the feedback gain adjuster 30 and the filter coefficient update section 31 that update the filter coefficient from the output of the equalization error detector 28 (which correspond to the equalization coefficient deciding unit).

Reference 2 describes a technique that the PLL circuit 5 extracts a frame sync pulse TMAX (which corresponds to a clock synchronized with an input signal) from an output of the equalizer circuit (waveform equalizer) 1, and it is easy for persons skilled in the art to apply this technique to the technique described in Reference 1.

Reference 3 describes the variable equalizer means that calculates a multiplication factor a(n) of taps (which corresponds to weighting), from the sum of constant tables A1 and A2 that have the same value on the left and right sides from the center of taps, for plural odd or even taps constituting the FIR filter, and constant tables A3 and A4 that have values opposite in sign on the left and right sides, and it is easy for persons skilled in the art to apply this technique to the technique described in Reference 1.

Supplemental Box

(To be used when the space in any of the preceding boxes is not sufficient)

Continuation of V.

The invention as defined in Claim 2 has no inventive step in view of References 1-6 cited in the International Search Report.

Reference 4 describes a technique of setting, in the initial stages of correcting the tap coefficients by the equalizer, an operation mode in which the tap coefficients are made coincide with each other for a combination of taps in symmetrical positions to stably vary the coefficients, and thereafter shifting to an operation mode that enables to set asymmetrical values.

Further, as seen in References 5 and 6, changing the operation mode after the tap coefficient of the equalization circuit is reset to the initial value before the PLL circuit is locked, to prevent conflict between adjustment of the equalization circuit and synchronization pull-in of the PLL circuit is a well-known technique.

Therefore, it is easy for persons skilled in the art to apply the technique described in Reference 4 to the technique described in Reference 1, to use the operation mode of symmetrically weighting the equalization coefficients before the PLL gets in a locked state.

The inventions as defined in Claims 3-10 are not described in any references cited in the International Search Report, nor obvious to persons skilled in the art.